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Closed Loop Control of an Interleaved Buck Converter with High Step-Down Conversion Ratio and Low Switch Voltage Stress

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Abstract: Interleaving can be thought of as a method of paralleling converters but it has got additional benefits to offer in addition to those obtained from conventional approaches of paralleling converters. Interleaved converters due to its simple structure and low control complexity are widely used in applications where non-isolation and high output current with low ripples are required. They have got certain drawbacks such as high cost and high switching losses and require high voltage rated devices. These drawbacks can be rectified by means of a new interleaved DC-DC converter in which two input capacitors are series-charged by the input voltage and parallel discharged for providing a much higher step-down conversion ratio. This paper employs capacitive voltage division principle for increasing the step-down conversion ratio and reducing voltage stresses of active switches. Thus lower voltage rating switches can be used to reduce switching losses and the overall efficiency is improved. Moreover, due to the charge balance of the blocking capacitor, the converter features automatic uniform current sharing characteristic of the interleaved phases without adding extra circuitry or complex control methods. The closed loop control of the paper is carried out using MATLAB R2012a environment and results are obtained. The closed loop control is given using a PI controller. Finally, a prototype circuit is implemented with 110 V input voltage and 5.5 V output voltage.

Keywords: IBC, interleaving technique, step-down conversion ratio, low switch voltage stress.

I. INTRODUCTION

Interleaving technique connects converter-converter in parallel to share the power flow between two or more conversion chains. It implies a reduction in the size, weight and volume of the inductors and capacitors. Also a proper control of the parallel converters reduces the ripple waveforms at the input and output of the power conversion system, which leads to a significant reduction of current and voltage ripples. Interleaving technique is used in some applications due to its advantages regarding filter reduction, dynamic response and power management. In applications where non-isolation, step-down conversion ratio, and high output current with low ripples are required, an interleaved buck converter (IBC) has received a lot of attention due to its simple structure and low control complexity [1]-[4]. However, in the conventional IBC shown in Fig. 1, all semiconductor devices suffer from the input voltage, and hence, high voltage devices rated above the input voltage should be used. High voltage rated devices have generally poor characteristics such as high cost, high on-resistance, severe reverse recovery, etc. In addition, the converter operates under hard switching condition. Thus, the cost becomes high and the efficiency becomes poor. However, higher switching frequencies increase the switching losses associated with turn-on, turn-off, and reverse recovery. Consequently, the efficiency is further deteriorated. Also, it experiences an extremely short duty cycle in the case of high-input and low-output voltage applications.

Due to the drawbacks of the conventional IBC a new mechanism was introduced which is the two phase extended mechanism.

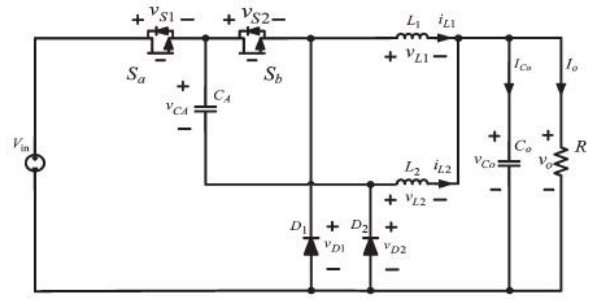

Fig. 1. Conventional IBC

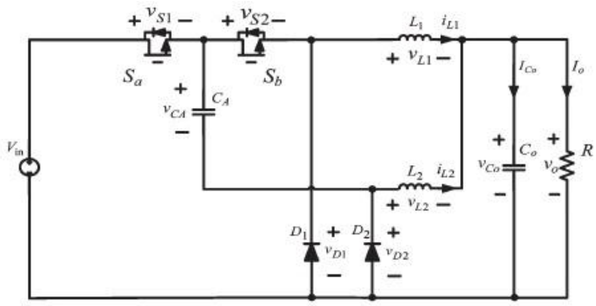

Fig. 2. Two Phase Extended IBC

In the two-phase extended IBC, as shown in Fig. 2, the two switches are connected in series and there is coupling capacitor in the power path [5]. This IBC operates at continuous conduction mode. So its current stress is low. They are efficient input voltage dividers which reduce the switching voltage and associated losses. However, the voltage stress of the input switch devices remains rather high. Therefore, we go for the modified IBC.

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In the modified IBC, the two input capacitors are series charged by input voltage and parallel discharged. Capacitive voltage division principle is employed here and by using this principle energy is stored in the blocking capacitors for increasing step down conversion ratio and for reduction of voltage stress of switches resulting in low switch voltage stress characteristics. Also, due to the charge balance of the blocking capacitor, uniform current sharing characteristics are obtained. So, extra circuitry or complex methods are not required.

II. CIRCUIT OPERATION

The modified IBC is shown in Fig. 3. It consists of two inductors, four active power switches, two diodes, and four capacitors. The main objectives of the four capacitors are: firstly, they are used to store energy as usual and secondly, based on the capacitive voltage division principle, they are used to reduce the voltage stress of active switches as well as to increase the step-down conversion ratio. Basically, the operating principle of the modified converter can be classified into four operating modes. The interleaved gating signals are given with a 180^0 phase shift.

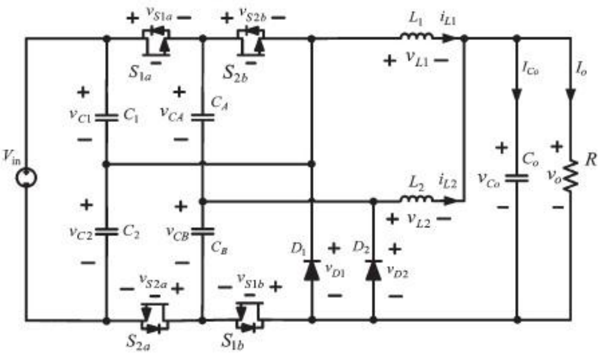

Fig. 3. Modified IBC

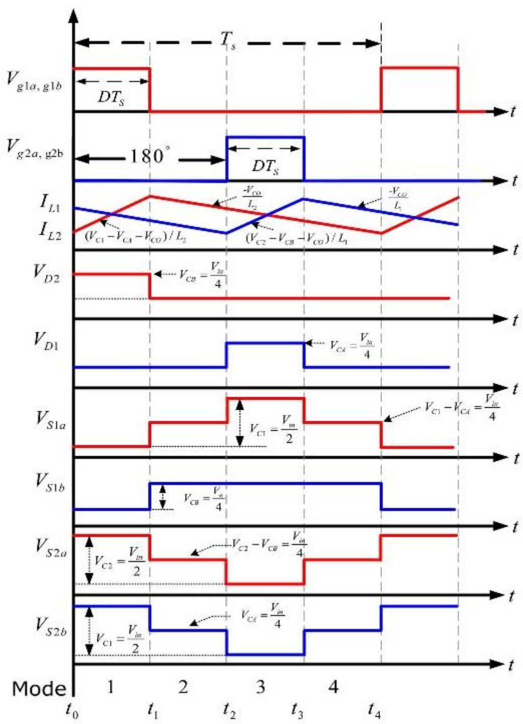

Fig. 4. Key operating waveforms of the new IBC

As the main objective is to obtain a high step-down conversion ratio and as such characteristic can only be achieved when the duty cycle is less than 0.5 and in CCM, hence the steady-state analysis is made only for this case. However, in DCM, as there is not enough energy transfer from the blocking capacitors to the inductors, output capacitor, and load side, it is not possible to get the charge balance of the blocking capacitor, then the automatic uniform current sharing property will be lost, and additional current-sharing control should be included.

For illustrating the operation of IBC, certain assumptions are made as follows:

1. All components are ideal components.
2. $C_1 = C_2$ and $C_A = C_B$.
3. System operating in CCM.

A. Mode 1 [t0 - t1]:

During this mode, S1a, S1b and D1 are turned on; S2a, S2b and D2 while are turned off. The corresponding equivalent circuit is shown in Fig. 5. During this mode, current iL1 free- wheels through D1, and L1 is releasing energy to the output load. However, current iL2 provides two separate current paths through CA and CB. The first path starts from C1, through S1a, CA, L2, CO and R, and

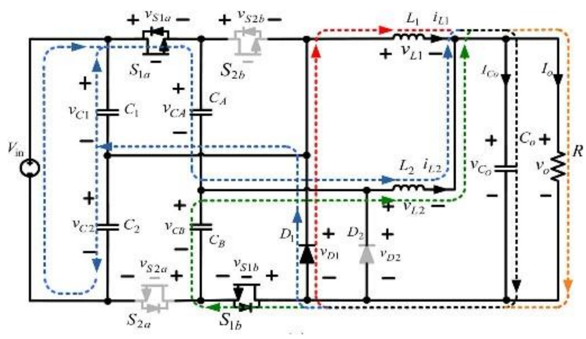

Fig. 5. Mode 1 operation

D1 and then back to C1 again. Hence, the stored energy of C1 is discharged to CA, L2, and output load. The second path starts from CB, through L2, CO and R, and S1b and then back to CB again. In other words, the stored energy of CB is discharged to L2 and output load. Therefore, during this mode, iL2 is increasing, and iL1 is decreasing as shown in Fig. 4.

B. Mode 2 [t1 - t2]:

During this mode, S1a, S1b, S2a, and S2b are turned off. The corresponding equivalent circuit is shown in Fig. 6. In this mode, both iL1 and iL2 are free-wheeling through D1and D2, respectively.

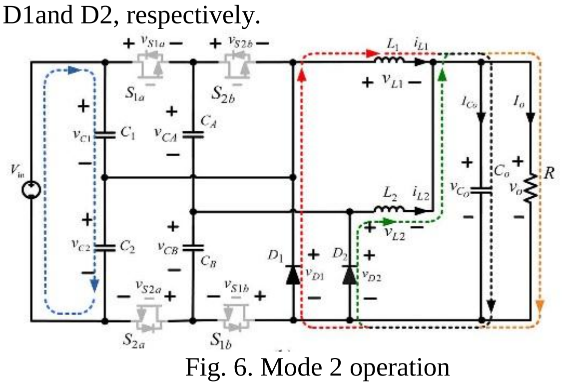

Fig. 6. Mode 2 operation

C. Mode 3 [t2 - t3]:

During this mode, S2a, S2b, and D2 are turned on, while S1a, S1b, and D1 are turned off. The corresponding equivalent circuit is shown in Fig. 7. During this mode, current iL2 is free- wheeling through D2 and L2 is releasing energy to the output load.

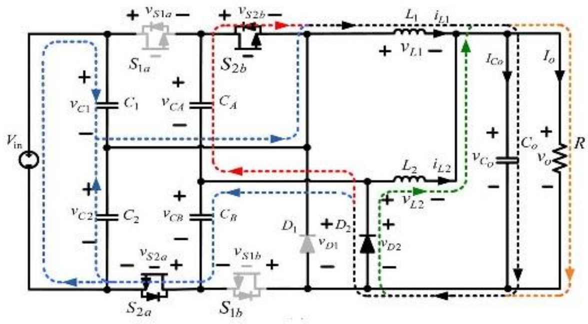

Fig. 7. Mode 3 operation

However, current iL1 provides two separate current paths through CA and CB. The first path starts from C2, through L1, CO and R, D2, CB, and S2a and then back to C2 again. Hence, the stored energy of C2 is discharged to CB, L1, and output load. The second path starts from CA, through S2b, L1, CO and R, and D2 and then back to CA again. In other words, the stored energy of CA is discharged to L1and output load. Therefore, during this mode, iL1 is increasing, and iL2 is decreasing as shown in Fig. 4.

D. Mode 4 [t3 - t4]:

For this operation mode, S1a, S1b, S2a, and S2b are turned off. The corresponding equivalent circuit is shown in Fig. 6, and its operation is the same as that of mode 2.

III.SIMULATION

The closed loop control of the modified IBC is shown in Fig. 8. Simulation is carried out using MATLAB R2012a environment. The input voltage, voltage waveforms across the switches and diodes, current waveforms of inductors, output voltage and output currents are obtained from the simulink model.

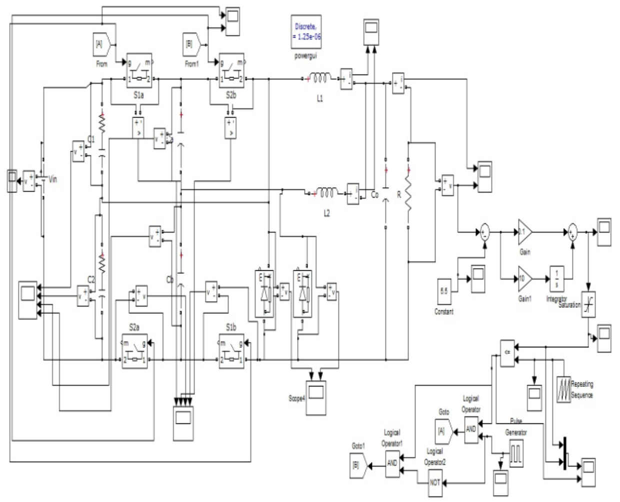

Fig. 8. Simulink model of the closed loop operation

The parameters given to the circuit are listed below:

V_{in}	110 V
D	0.2
V_O	5.5 V
L1, L2	250 µH
C_O, C_1, C_2	250 µf
C_A C_B	10 µf
Fs	40 kHz
Kp	0.1
Ki	10

Different equations used for obtaining values in the simulation are:

$$V_O = \frac{D}{4} V_S$$

$$\Delta I_{Lripple} = \frac{V_O}{L}(1-D)T_S$$

$$\Delta V_{CBripple} = \frac{I_O D}{2 C_B f_S}$$

$$\Delta V_{COripple} = \frac{I_O D}{2 C_O f_S}$$

where, D is the duty ratio, Vin is the input voltage, ILripple is the inductor ripple current, VCBripple and VC0ripp VC0ripple are the capacitor ripple currents, V0 is the output voltage and fs is the switching frequency.

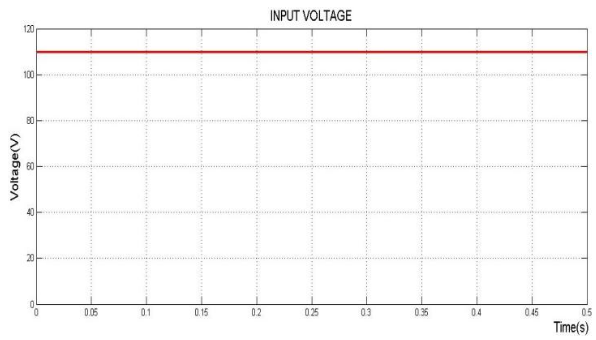

Fig. 9. Input voltage

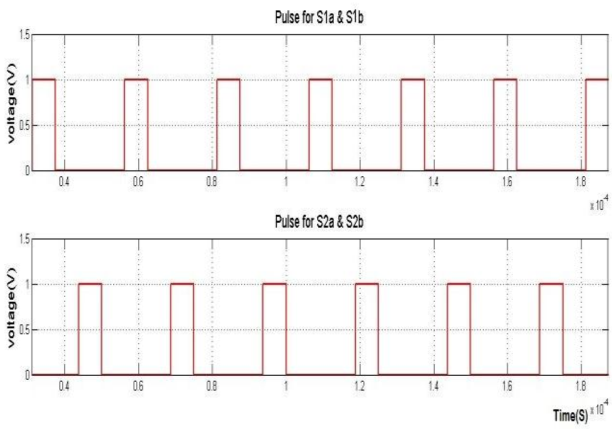

Fig. 10. Pulses for the switches

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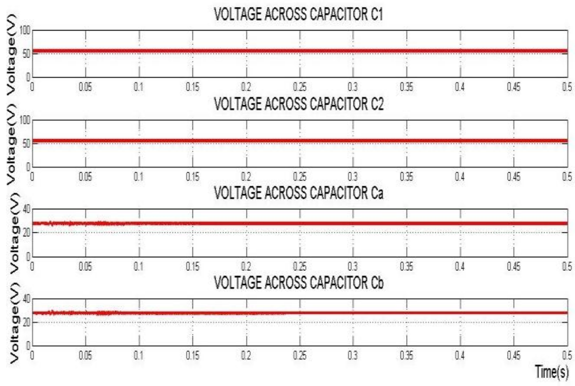

Fig. 11. Voltage across the capacitors

The waveforms obtained from simulation are shown. Input voltage is 110V, output voltage is 5.5V, output current is 1.1A. The step response of the closed loop control is shown in Fig. 16. which implies the proper working of the closed loop. Lower limit is 5.5 and upper limit is 6.5.

Fig. 9-15 shows the input voltage, the output voltage; output current, inductor currents, voltage across diodes, voltage across capacitors, gate pulses which are of 180^0 phase shift and the voltage across switches for a duty ratio of 0.25. The inductor currents (Fig. 14) are identical to the theoretical waveform given in Fig. 4. The voltage strain of switches S1a, S2aand S2b is only one half of the input source voltage and that of S1b is one fourth of the input source voltage (Fig. 13), which is one of the merits of the converter.

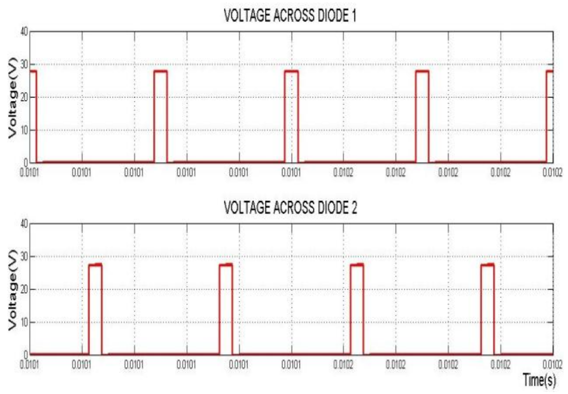

Fig. 12. Voltage across the diodes

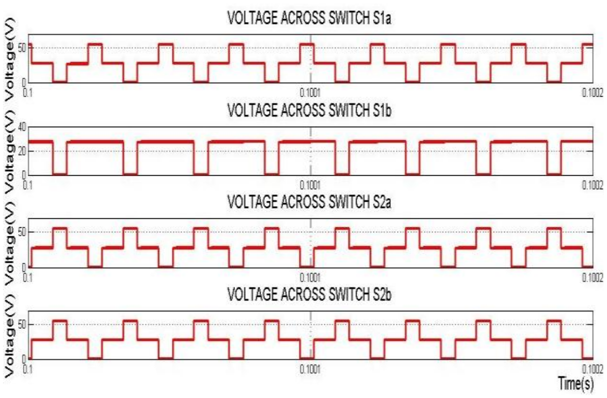

Fig. 13. Voltage across the switches

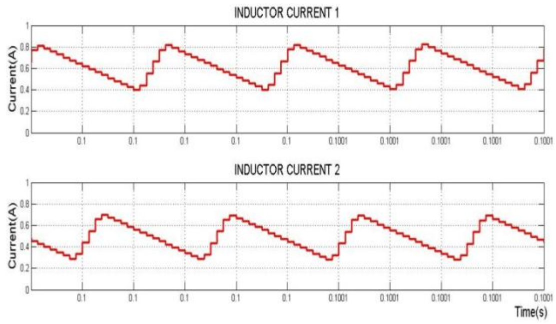

Fig. 14. Current through the inductors

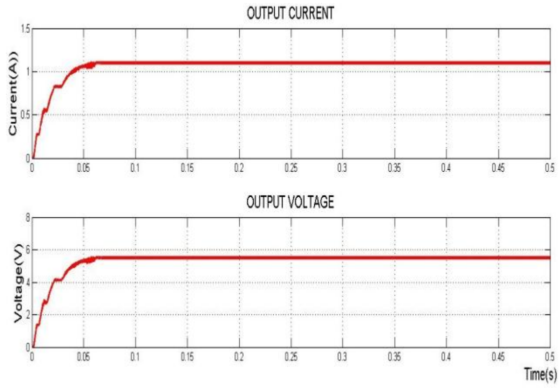

Fig. 15. Output current and output voltage

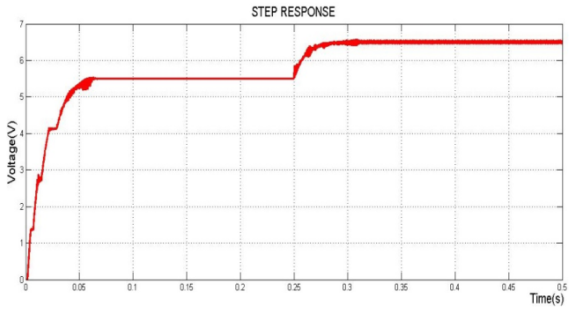

Fig. 16. Step response

IV. HARDWARE

Fig. 17. shows the closed loop control (block diagram) of the IBC.

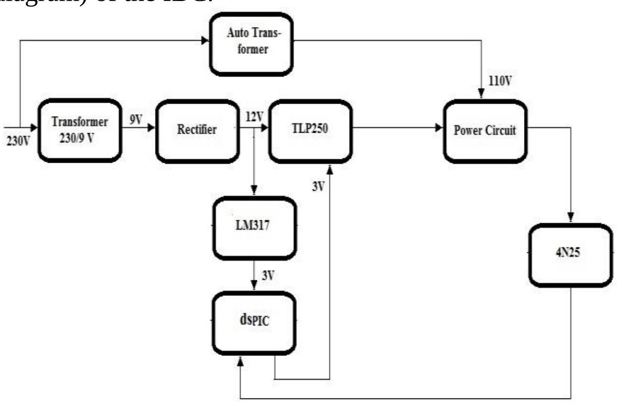

Fig. 17. Block diagram of the closed loop control of IBC

The supply 230V is given to a step down transformer to obtain an output of 9V. This 9V is given to a rectifier to get 12V output which is the supply for the gate driver IC TLP250. This 12V supply is also given to the voltage regulator IC LM317. The output of LM317 is 3V which is

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the supply for dsPIC. The dsPIC is connected to TLP250 which gives the required gate signals and is fed to the power circuit. The input to the power circuit is 110V, and is obtained from the supply using an auto-transformer. There is a feedback IC 4N25. The output voltage is given to this IC and fed back to TLP250 such that the output voltage remains constant against any variations in the input.

The experimental setup of the hardware is shown in Fig. 18. The specifications of the components used in the power circuit are given in table below. The waveforms obtained from the hardware implementation are shown in Fig. 19-28.

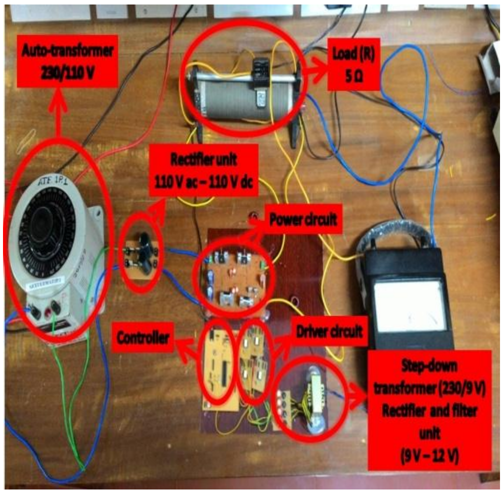

Fig. 18. Experimental setup

Fig. 19. Input voltage

Fig. 20. Pulses for switches S1a and S1b

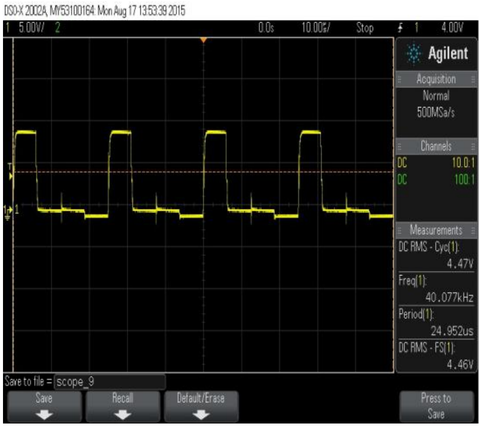

Fig. 21. Pulses for switches S2a and S2b

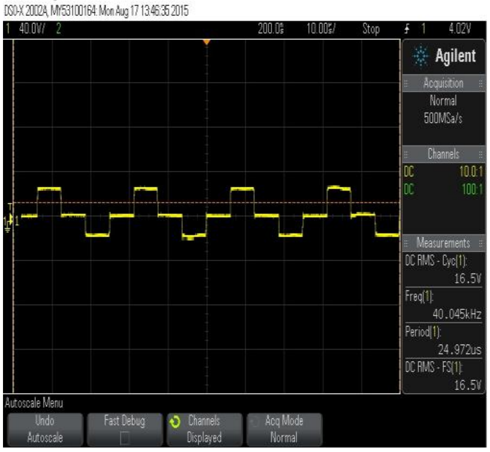

Fig. 22. Voltage across switch S1a

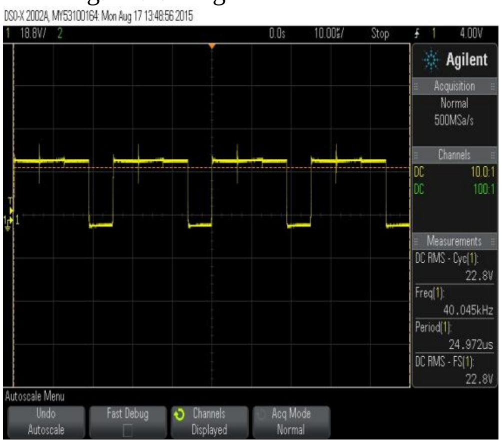

Fig. 23. Voltage across switch S1b

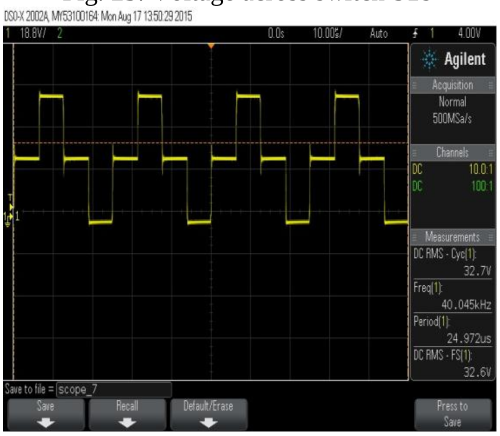

Fig. 24. Voltage across switch S2a

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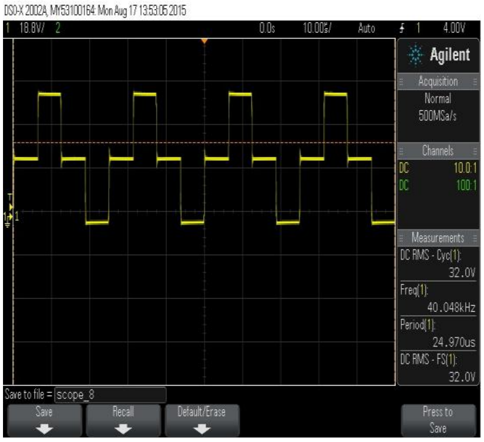

Fig. 25. Voltage across switch S2b

Fig. 26. Voltage across diode 1

Fig. 27. Voltage across diode 2

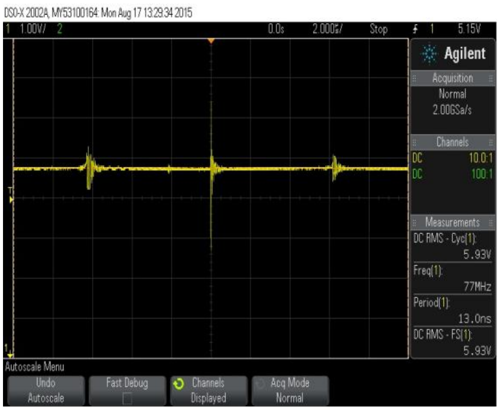

Fig. 28. Output voltage

Fig. 19 shows the input voltage, 110 V. Fig. 20 shows the pulse for switches S1a and S1b. The switching frequency given is 40 kHz. Fig. 21 shows the pulse for switches S2a and S2b. Fig. 22 shows the voltage across switch S1a. The peak value is obtained as 23.3 V. Fig. 23 shows the voltage across switch S1b. The peak value is obtained as 32.2 V. Fig. 24 shows the voltage across switch S2a. The peak value is obtained as 46 V. Fig. 25 shows the voltage across switch S2b. The peak value is obtained as 45 V. Fig. 26 and Fig. 27 shows the voltage across diodes D1 and D2. The peak value is obtained as 20.36 V. Fig. 28 shows the output voltage and is obtained as 5.93 V.

Comparing these experimental results with the theoretical waveforms, we can see the shapes of all the waveforms are identical to the theoretical waveforms. Comparing with the simulation results, we can see the shapes of all the waveforms are same and the voltage amplitude is almost same as that obtained in the simulation results. For S1a, the voltage from simulation is 55 V and that from hardware is 23.3 V and the percentage error is 31.7%. For S2a and S2b, the voltage from simulation is 55 V and that from hardware is almost 46 V and 45 V; thus the percentage error is 9% and 10%. For S1b, the voltage from simulation is 27.5 V and that from hardware is 32.2 V and the percentage error is 4.7%. For D1 and D2, the voltage from simulation is 27.5 V and that from hardware is 20.36 V and the percentage error is 7.14%.

V. CONCLUSION

Here, a new transformerless interleaved high step-down conversion ratio dc-dc converter with low switch voltage stress was discussed. The two input capacitors are series- charged by the input voltage and parallel discharged by a new two-phase IBC for providing a much higher step-down conversion ratio without adopting an extreme short duty cycle. Based on the capacitive voltage division, the main objectives of the new voltage-divider circuit in the converter are both storing energy in the blocking capacitors for increasing the step-down conversion ratio and reducing voltage stresses of active switches. As a result, the modified converter topology possesses the low switch voltage stress characteristic. This will allow one to choose lower voltage rating MOSFETs to reduce both switching and conduction losses, and the overall efficiency is consequently improved. Moreover, due to the charge balance of the blocking capacitor, the converter features automatic uniform current sharing characteristic of the interleaved phases without adding extra circuitry or complex control methods.

REFERENCES

[1] C. Garcia, P. Zumel, A. D. Castro, and J. A. Cobos, “Automotive DCDC bidirectional converter made with many interleaved buck stages”, IEEE Trans. Power Electron., vol. 21, no. 21, pp. 578-586, May 2006.
[2] R. L. Lin, C. C. Hsu, and S. K. Changchien, “Interleavedfour-phase buck-based current source with isolatedenergy-recovery scheme for electrical discharge machine”, IEEE Trans. Power Electron., vol. 24, no. 7, pp. 2249-2258, Jul. 2009.
[3] Y. C. Chuang, “High-efficiency ZCS buck converter for rechargeable batteries”, IEEE Trans. Ind. Electron., vol. 57, no. 7, pp. 2463-2472, Jul. 2010.
[4] C. S.Moo, Y. J. Chen, H. L. Cheng, and Y. C. Hsieh, “Twin-buckconverter with zero-voltage-transition”, IEEE Trans. Ind. Electron., vol. 58, no. 6, pp. 2366-2371, Jun. 2011.
[5] I.-O. Lee, S.-Y. Cho, and G.-W. Moon, “Interleaved buck converter having low switching losses and improved step-down conversion ratio”, IEEE Trans. Power Electron., vol. 27, no. 8, pp. 3664-3675, Aug. 2012.